Solar Photovoltaic Technology

J. N. Roy

Abstract There is all around focus on the development of renewable energy due to energy security, climate change and energy access. Solar photovoltaic deals with conversion of sunlight into electricity. Understanding the available energy resources at Earth's surface that can be used for this conversion is important. The single- and multi-crystalline silicon solar cells dominate the present PV market and occupy >85% of it. Advancements are continuously being made and efficiency of the most widely used cells using c-Si cells now touching up to 20%. Higher efficiency cells use III–V compound semiconductors. Commercial efficiency of more than 30% is now routinely achieved using high-efficiency multi-junction (MJ) III–V cells. Due to cost consideration, these cells are primarily being used in space. Concentrated Photovoltaic (CPV) using high-efficiency MJ cells are used in terrestrial application. Thin-film solar cell is relatively new technology and now occupies about 10% of PV market. The present conversion efficiencies of a-Si thin film solar cells are 8–10% (stabilized) and that of micromorph 9–11% (stabilized) at the production level. Amongst the compound semiconductor, thin-film solar cells CdTe are being produced on mass scale. The conversion efficiency is about 10%. For CIGS the production technology is not yet fully matured. There are several new types of solar cell technologies attracting attention. Dye-sensitized solar cell (DSSC) mimics photosynthesis process. The efficiency achieved is 15–16% in the laboratory scale. However, stability is a problem which is standing in the way of its commercial production. Organic and polymer-based solar cells have not been able to make much progress in terms of efficiency and stability. The other important R&D activities which are going to enhance the conversion efficiencies of solar cells are based on better light management so that current from the cell goes up. For this nanotechnology involving nanostructures are being used.

Keywords Solar cell · Solar resources · Concentrated photovoltaic (CPV) Band gap · Equivalent circuit · Maximum power point (MPP)

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1 Introduction

There is all around focus on the development of renewable energy due to energy security, climate change and energy access [1–5]. Solar photovoltaic deals with direct conversion of sunlight into electricity. Governments across the world realized the importance of solar power and many countries have introduced feed-in tariffs, capital subsidies and incentives for productions to promote wider adoption and advancement of solar PV. Renewable initiatives, particularly solar PV, have picked up pace in India. The Jawaharlal Nehru National Solar Mission (JNNSM) is a major initiative of the Government of India to give an impetus to the domestic solar power industry. Several State Governments have announced independent policies in solar PV.

The single- and multi-crystalline silicon solar cells [6] dominate the present PV market and occupy about 90% of it. Thin-film solar cell [7–9] is relatively new technology and now occupies about 10% of PV market. Amongst the compound semiconductor thin-film solar cells, CdTe [10–12] and CIGS [13, 14] have matured and are used in production. There are several new types of solar cell technologies attracting attention. Dye-sensitized solar cell (DSSC) [15] mimics photosynthesis process. Although it is a cost-effective solution, stability is a major issue and in the way of its commercial production. Organic- and polymer-based solar cells have not been able to make much progress in terms of efficiency and stability. Recently, a new type of solar cell, known as perovskite solar cell [16], has been discovered and is generating lot of attention. High-efficiency III–V solar cell exhibits very high efficiency. Due to much higher cost, use of such solar cells is limited to space and terrestrial concentrated photovoltaic (CPV) applications.

2 Solar Resources

Sun is a star and provides most of energy available at Earth. The energy generation in the Sun is due to nuclear fusion, and this energy is transmitted in all directions. The total power emitted can be estimated as about 3.9×10^{26} W by assuming Sun as a black body with a surface temperature of about 5800 K. A small part of this energy is intercepted by Earth as decided by the solid angle subtended from the Sun. This can be estimated as about 1370 W/m^2 outside the Earth's atmosphere. This is known as solar constant and has small variation throughout the year, as distance between the Sun and the Earth varies. Further attenuation happens due to absorption of portion of the energy as it travels through atmosphere. Therefore, the power received at the surface of the Earth, also known as "irradiance", is lower than the solar constant and varies from place to place depending on the altitude. The irradiance value also changes throughout the day at a particular place as the travel path of the sunrays varies. This is shown in Fig. 1. Sunrays travel different

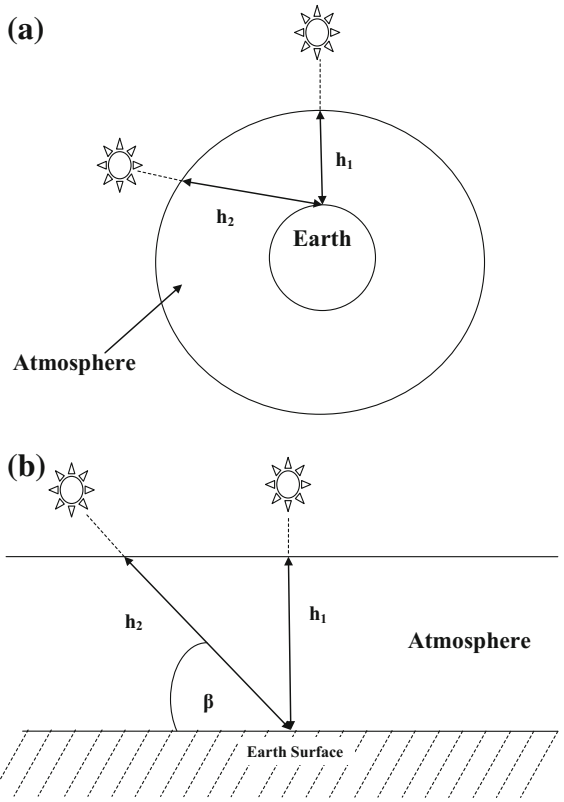


Fig. 1 **a** During two different times of a particular day, Sunrays travelling different distance through atmosphere to reach at a particular point on Earth surface. **b** Simplified version of (**a**) assuming flat Earth at the location of interest

distances through the atmosphere at two different times of the day to reach a particular point of the Earth as shown in Fig. 1a. A simplified version is shown in Fig. 1b assuming the Earth is flat at the location of interest. It can be seen that h_1 is the minimum possible distance. This happens when the Sun is directly overhead, which is also known as Zenith position. At any other location of the Sun, the distance travelled by the Sunrays through the atmosphere is always larger.

An important term, Air Mass (AM), is defined to quantify this. Sometime this is also called atmospheric mass (AM). AM0 corresponds to outside the atmosphere. The reference point at the Earth surface is AM1, when the Sun is at Zenith. At any other time of the day the air mass is defined as given in Eq. 1.

$$\text{Air Mass } m = (h_2/h_1) = (1/\sin\beta) \tag{1}$$

β is the altitude of the Sun. AM1.5 corresponds to $\beta \approx 42^\circ$, which is also approximated as the average irradiance received during the entire day at that particular location.

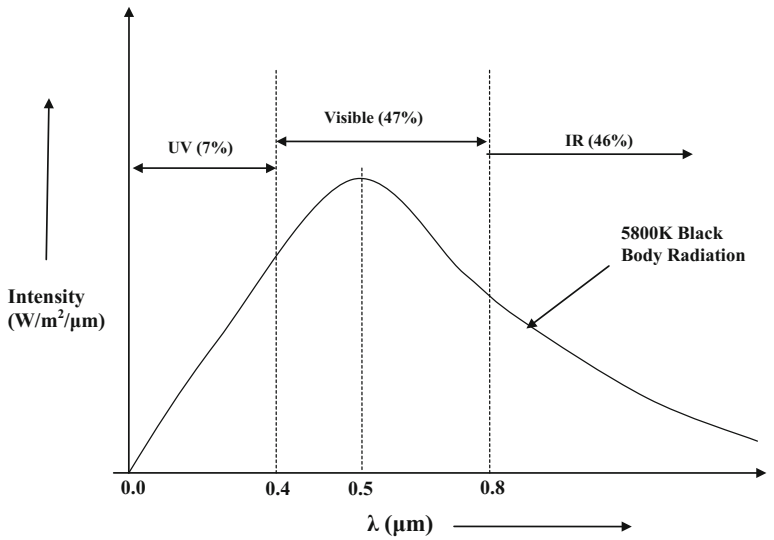


Fig. 2 Spectral distribution of 5800 K black body. The radiation received by the Earth at outside atmosphere (AM0) is also similar

The energy emitted by Sun has a spectral distribution corresponding to a black-body emitter having a temperature of 5800 K as shown in Fig. 2. The actual extraterrestrial radiation (AM0) closely resembles the spectrum shown in Fig. 2. The peak intensity is at $\lambda = 0.5$ μm, which corresponds to green part of visible spectrum. The total energy is roughly divided in ultraviolet (UV: $\lambda < 0.4$ μm): 7%, visible (0.4 μm $< \lambda <$ 0.8 μm): 47% and infrared (IR: $\lambda > 0.8$ μm): 46%. The spectral distribution of intensity gets modified (not shown) as it travels through the atmosphere. The energy distribution also gets modified depending on altitude and air mass. The rough energy distribution at AM1.5 is 2.0% UV, 54% visible and 44% IR.

The total irradiance available at Earth's surface consists of mainly three parts. The major part is known as direct radiation denoted by direct normal incident (DNI). This is also known as global (G) part of the total irradiance. During cloudy weather, DNI is zero. Any collector receiving the direct radiation will receive full DNI, denoted here as I_{DG}, when the Sunrays are falling perpendicular on the collector surface as shown in Fig. 3. At any other Sun angle, the collector receive irradiance of $I_{DC} = I_{DG} \cos \theta$ as shown in Fig. 2. The collector can be a solar photovoltaic (SPV) module.

The other important portion of the irradiance received by Earth's surface is known as diffused radiation generated due to scattering of sunlight due to cloud, dust particles or even constituent gases in the atmosphere. During a cloudy day, although the DNI is zero, there are diffused radiations. Diffused radiation is modelled as if it is coming from all directions uniformly as shown in Fig. 4. The sky

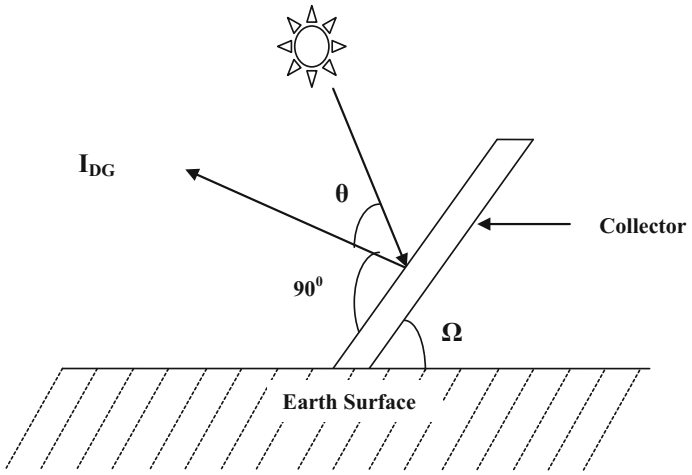


Fig. 3 Collector receiving direct radiation

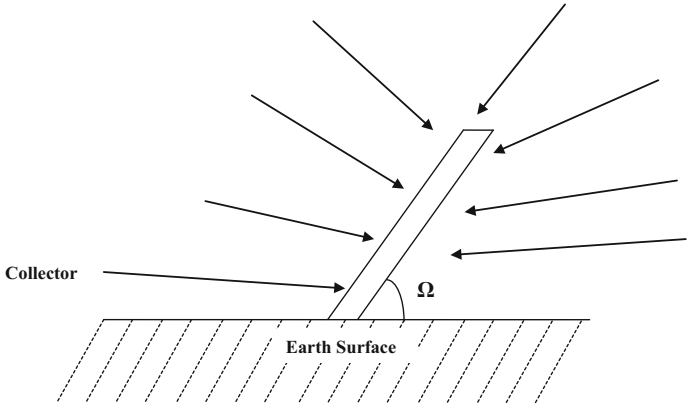


Fig. 4 Collector receiving diffused radiation

diffusivity factor (d) decides the amount of total diffused radiation (I_S), which eventually decided by the DNI. A simplistic model is shown in Eq. 2.

$$I_S = d\, I_{DG} \tag{2}$$

The total diffused radiation received by the collector (I_{SC}) depends on the tilt angle Ω (see Fig. 3) and it is given as shown in Eq. 4.

$$I_{SC} = d\, I_{DG}(1 + \cos\Omega)/2 \tag{3}$$

In case the collector is kept horizontal to the ground, the entire diffused radiation will be available to the collector. On the other hand, in case the collector is perpendicular to the surface, the amount of diffused radiation received is 50% of the total.

Reflected radiation forms another small portion of the total radiation received by the collector. The reflection can be from the ground, adjacent mountain which may be covered by the snow and other structures such as buildings. This is very small and mainly depend on the ground material on which the collector are installed and surroundings.

The total radiation received by the collector is the sum total of direct and diffused radiation assuming the reflected radiation is negligible. On an average, the reflected radiation is about 0.5–1.5% depending on the location and surroundings. The direct radiation forms the major part of the total radiation, about 75%, if long-term average (e.g. a year) of a particular location is considered. Diffused radiation, about 25%, forms the other part. These figures will vary based on the climatic conditions of the location. For example, for a tropical country like India, the figures mentioned (75% direct and 25% diffused) would be close. Another place where there are more cloudy days, the diffused radiation contribution will be more. Estimation of direct and diffused radiation separately is important due to several reasons. Tracking-based SPV system only improves the direct radiation collection as the sunrays fall perpendicular to the collector most of the time. However, the amount of diffused radiation remains same as compared to a fixed SPV installation. In concentrated photovoltaic (CPV) [17], it is possible to only use direct part of the radiation to be concentrated to a point. Some SPV technologies, e.g. thin film amorphous silicon, diffused irradiance performance is better.

3 Photovoltaic Materials

Electrical conductivity of inorganic materials mainly gets decided by the nature of bonding prevailing amongst the constituent atoms or molecules. Semiconductor materials are formed due to strong covalent bond between constituent atoms or molecules. Elemental semiconductors are Si, Ge, etc. from group IV of periodic table and also compound semiconductors formed by two elements, one from group III and another from group V. Examples of compound semiconductors are GaAs, InP, etc. Compounds formed between one element of group II and another element of group VI, e.g. CdTe, are also semiconductor. In general, semiconductor materials have average valence electrons count as four. Other combinations such as Cu (group I), In (group III) can substitute Cd (group II) and if combined with group VI element such as Se forms semiconductor (Copper Indium Selenide-CIS). Band gap, which is introduced later, can be adjusted by using multiple elements from the same group retaining the basic requirement as discussed above. $Ga_xIn_{1-x}As$, $Ga_xIn_{1-x}P$, $Ga_xIn_{1-x}As_yP_{1-y}$ are examples of such semiconductors. Band gap can be tailored by varying x and y.

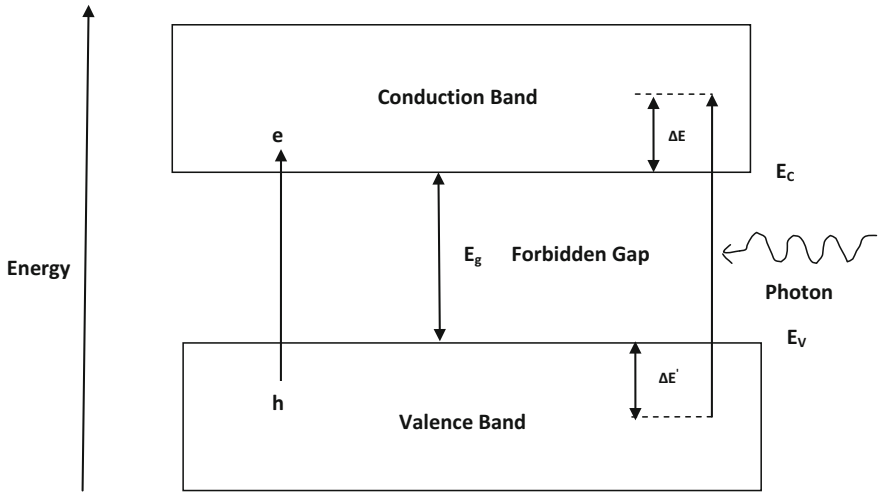


Fig. 5 Semiconductor band structure. E_V: Top of the valence band, E_C: bottom of the conduction band, E_g: band gap, h: hole, e: electron

The semiconductor [18] has a characteristics band structure as shown in Fig. 5. The valence band has allowed closely spaced energy levels (not shown) which are known as density of states. The number of such states is really large; in the order of $10^{23}/cm^3$. The highest allowed energy level in the valence band, also known as top of valence band, is denoted as E_V. Allowed energy levels do not necessarily mean that those are occupied by carriers, electron in this case. However, for intrinsic semiconductor at 0 K, all the available energy levels in the valence band are occupied by electrons. The free carrier concentration is zero and the material behaves like perfect insulator with zero conductivity.

The conduction band also has allowed closely spaced energy levels (not shown). The density of such states is also large: in the order of $10^{23}/cm^3$. The lowest allowed energy level in the conduction band, also known as bottom of the conduction band, is denoted as E_C. None of the energy levels in the conduction band are occupied by electrons for an intrinsic semiconductor at 0 K. There are no allowed energy levels in between top of the valence band and bottom of the conduction band. This is known as forbidden gap or band gap (E_g). Exciting electrons from the valence band to the conduction band require a minimum energy of E_g. At temperature other than 0 K, some of the carriers at the valence band acquire energy greater than E_g and get excited to the conduction band. Such carriers are called intrinsic carrier concentration, which strongly depends on temperature and bang gap. If one electron gets excited from the valence band to conduction band, there is a corresponding hole which gets generated in the valence band as shown in Fig. 5. Both type of free carriers (electron and hole) can contribute to conductivity. Intrinsic carrier concentration for semiconductor materials is small. For example, for silicon with a band gap of about 1.1 eV, the intrinsic carrier concentration is about $1 \times 10^{10}/cm^3$.

It is possible to increase the free carrier concentration of electrons and holes by doping elements from group V and group III, respectively. These are known as n-type extrinsic semiconductor or p-type extrinsic semiconductor with extrinsic carrier concentrations decided by the level of doping, i.e. doping concentrations. The conductivity of the typical extrinsic semiconductors is therefore not as high as metal but much higher than insulator.

Photovoltaic devices use the energy of photons (see Fig. 2) to excite additional electrons from the valence band to the conduction band creating e–h pairs as shown in Fig. 5. The excitation and creation of additional e–h happens only if the energy ($E = h\upsilon = hc/\lambda$) of the photon is greater than the band gap. The photons having energy more than the band gap of the material are absorbed and create e–h pairs as shown in Fig. 5. The other photons with lower than this energy is simply passed through the material without contributing any e–h pairs generation. This is known as cut-off wavelength which is given as $\lambda_{\text{cut-off}} = hc/E_g$ or $\lambda_{\text{cut-off}}$ (in μm) $\approx$ 1.24 eV/E_g (in eV). For example, this cut-off wavelength for silicon is about 1.13 μm with a band gap of about 1.1 eV. The additional e–h pairs generated effectively increase carrier which can be used for photoconductivity or electricity generation. Electricity generation requires a semiconductor device (p–n junction diode) which is discussed later.

The photoconductivity can be observed in a standard electrical circuit in which semiconductor material is used as a resistor. As the photons are absorbed by the semiconductor material and create additional carriers (e–h pairs), the resistance decreases resulting in higher current. However, this cannot be used to generate electricity. In case no external electric field in the form of voltage is applied, these photon-induced carriers are not separated from each other and recombine eventually without contributing to any current. The photo-generated carriers can be separated by creating an internal field. This is done by using a p–n junction made by n-type and p-type semiconductor material. The band diagram and the internal field are shown in Fig. 6. The photon-generated electron-hole pairs get separated due to internal electric field (φ_B).

The solar cell is essentially a p–n junction diode made of semiconductor material. Due to absorption of photons, e–h pairs are created and separated by the internal field of the p–n junction diode generating the electric power. These carriers can flow through the external load connected to the p–n diode. It is now important to understand the power, which is a product of voltage (V) and current (I). The current (I) will be decided by the amount of additional carriers generated due to irradiance and the voltage is decided by the potential energy of these carriers.

The total additional carriers generated due to irradiance depend on the spectral response and the band gap of the material. The spectral response curve is reproduced in Fig. 7. The total power of the irradiance as depicted in Figs. 2 and 7 can be estimated as the area under the entire curve. However, only a portion of this power is absorbed depending on the band gap of the material. For example, for a band gap of E_{g1}, the cut-off wavelength ($\lambda_{\text{cut-off 1}}$) is about (1.24/$E_{g1}$) μm as shown in Fig. 7. The photons having wavelength of $\lambda_{\text{cut-off 1}}$ and below will be absorbed by the material. This can be estimated as the area of the curve between $\lambda = 0$ and

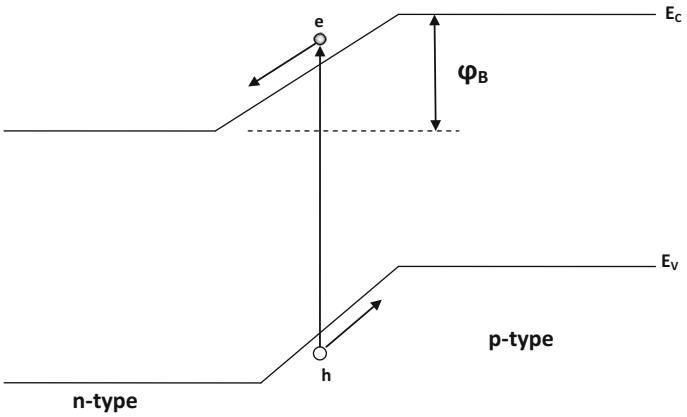


Fig. 6 Electron-hole pair separation due to potential barrier (φ_B) in p–n junction diode

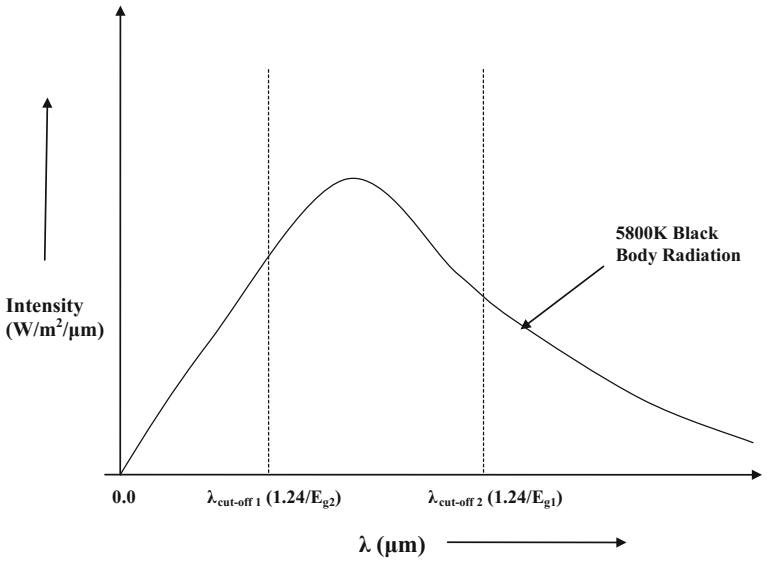


Fig. 7 Spectral response of radiation received by the Earth and the cut-off wavelengths

$\lambda = \lambda_{\text{cut-off 1}}$. Rest of the power, which falls on the right side of the $\lambda_{\text{cut-off 1}}$ curve is not absorbed and therefore does not contribute to carrier generation. As the band gap increases, the power which is absorbed by the material reduces. The material with band gap E_{g2}, which is higher than E_{g1}, absorbs less power as the area of the curve between λ and $\lambda_{\text{cut-off 2}}$ is lesser. It is clear therefore that the number of carriers generated due to absorbed irradiance depends on the band gap of material. The actual number of carriers generated can be estimated from the spectral response

knowing the total number of photons absorbed assuming one e–h pair is generated per one absorbed photon. This decides the current (I_L) produced by the photovoltaic device, which is also known as short-circuit current (I_{SC}). More about the short-circuit current are discussed later. It may be noted that the current produced by a photovoltaic device decreases as band gap increases.

The potential energy of the photo-generated carriers, which decides the voltage of the photovoltaic device, also depends on band gap. As shown in Fig. 5, the energy of the photon ($\lambda < \lambda_{cut\text{-}off}$) gets transferred to the electron in the valence band which then gets excited to the conduction band. Although the initial potential energy of the excited carrier is equal to the energy of the photon, ultimately it gets settled to the bottom of conduction band (top of the valence band for hole) by losing some energy as shown in Fig. 5. The total energy loss for e–h pair is ($\Delta E + \Delta E'$). This energy is lost and gets converted to heat. The voltage of the photovoltaic device therefore gets decided by the band gap. More the band gap more is the voltage.

The output power (P) of the photovoltaic device is the product of current (I) and voltage (V). The band gap of the material therefore decides the output power. As the band gap is increased from low to high, the current decreases but voltage increases. Limiting cases are $E_g \to 0$ ($I \to \infty$, $V \to 0$, and $P \to 0$) and $E_g \to \infty$ ($I \to 0$, $V \to \infty$, and $P \to 0$). There is then an ideal band gap which gives the maximum output power. The efficiency of the photovoltaic device is defined as (output power/input power). The input power is given by the entire curve of Figs. 2 and 7. The output power is less than the input power as some part of the spectrum gets unutilized due to $\lambda_{cut\text{-}off}$ issue and also due to the loss of ($\Delta E + \Delta E'$) as discussed earlier. The theoretical limit of the efficiency is calculated based on the above considerations. The practical efficiency obtained is less than the theoretical maximum due to several other factors, which are taken up later. The efficiency versus band gap plot is shown in Fig. 8. The maximum efficiency occurs at about $E_g = 1.45$ eV. Silicon has a theoretical efficiency of about 28%.

The higher theoretical efficiency can be achieved using multi-junction device. These are known as multi-junction (MJ) [19] or tandem [20] solar cells. Solar cells made using III–V compounds or amorphous silicon uses this technology. MJ or tandem solar cells use larger portion of the solar spectrum more efficiently by employing multiple semiconductor layers with different band gaps. Each layer absorbs different portions of the spectrum capturing more number of photons. This can be explained with the help of Fig. 9. The top layer (layer 3) absorbs the photons with energy more than the band gap energy (E_{g3}) and allows the lower energy photons to pass through. Layer 2 absorbs photons having energy between E_{g2} and E_{g3}. Similarly, in layer 3, photons having energy between E_{g2} and E_{g1} is absorbed.

It is possible to absorb all the photons having energy higher than E_{g1} by layer 1 alone. However, there is extra loss of energy in single-junction structure. The excess energy of a photon with reference to the band gap energy is lost mainly due to heat as explained earlier ($\Delta E + \Delta E'$). This loss is minimized by using MJ (tandem) structure. The voltages which are determined by the band gap is highest for cell 3 (V_3) and lowest for cell 1 (V_1). The open-circuit voltage of cell 2 (V_2) lies

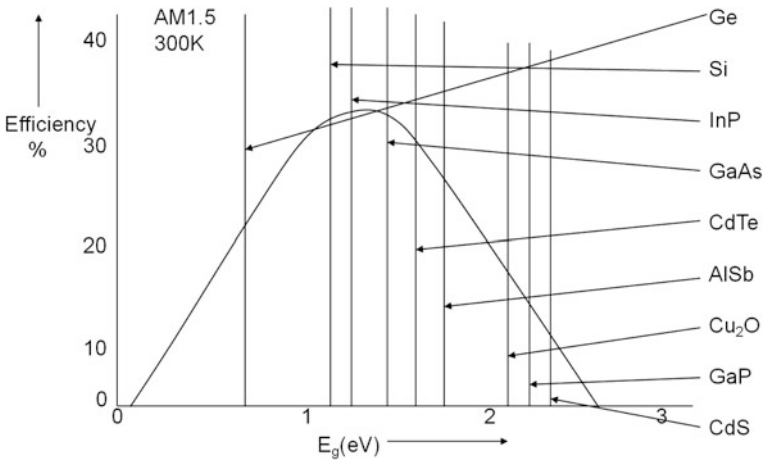
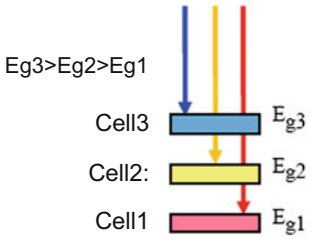


Fig. 8 Ideal (theoretical) efficiency of photovoltaic device as a function of band gap of the material. Maximum efficiency is at band gap of about 1.45 eV

Fig. 9 Three stacked materials absorbing larger part of the spectrum



in between. As the cells are connected in series, the effective open-circuit voltage of the MJ cell is the sum of these three voltages ($V_1 + V_2 + V_3$). The layers are to be carefully designed to have same short-circuit current (I_{SC}) for all the three cells as they are connected in series. Otherwise, the effective current is decided by the lowest current and there are losses of photo-generated carriers due to internal flow of current in the cell having lower current.

The band gap adjustment of the III–V compound semiconductor are done using ternary (e.g. $In_xGa_{1-x}P$) or quaternary (e.g. $In_xGa_{1-x}As_yP_{1-y}$) compounds by varying x or/and y. The band gap of amorphous silicon (a-Si) can be varied by incorporating germanium (a-Si:Ge) and carbon (a-Si:C).

The organic solar cells work on different principle as compared to inorganic solar cells described above. The photons absorbs by the organic materials generates excitons. These excitons are responsible for electrical conductions. The concept of valence band and conduction band are also not applicable in organic material. Instead, the highest molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) are equivalent to valence and conduction bands. The detail description of the organic photovoltaic is out of the scope of this chapter.

4 Electrical Characteristics of Photovoltaic Devices (Solar Cells)

The cross section of a p–n junction diode acting as a solar cell is shown in Fig. 10. The photo-generated carriers denoted by + for hole and—for electron get separated due to internal electric field in the depletion region and flow through the load generating current. The current is decided by the amount of photons absorbed and the band gap of the material as discussed earlier. The spectral response of the solar cell is essentially decided by the spectral response of the material used to make the solar cells. The details have been discussed in Sect. 3.

The symbolic circuit representation of Fig. 10 is shown in Fig. 11 which is also known as equivalent circuit. Figure 11a represent the equivalent circuit under no irradiance. Under irradiance and due to the internal field of the diode, a photo-generated current (I_L) gets established and acts as current source. This current

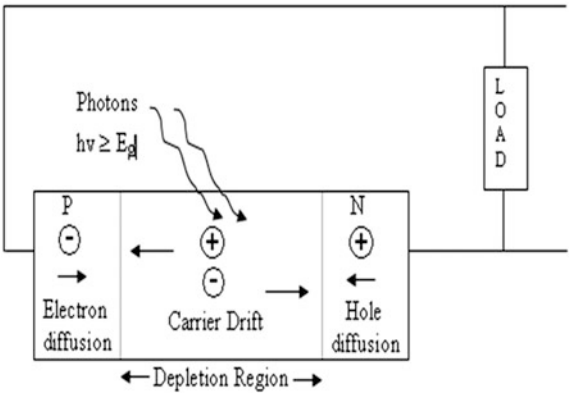


Fig. 10 Cross section of a p–n junction diode acting as a solar cell

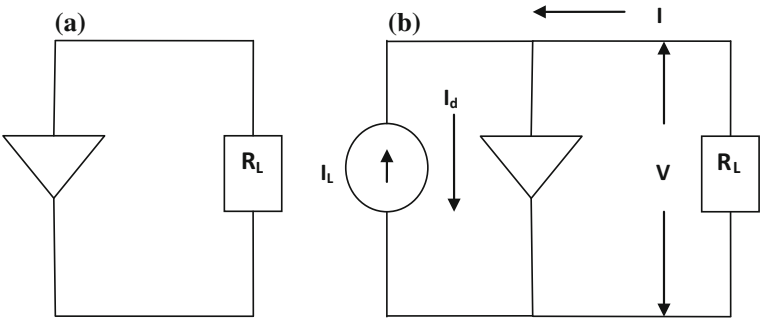


Fig. 11 **a** Ideal equivalent circuit in dark. **b** Ideal equivalent circuit under irradiance

flows through the load (R_L) and also through the diode. The diode current (I_d) which is given by Eq. 4 depends on the voltage (V) developed across it.

$$I_d = I_S\left(e^{qV/kT} - 1\right) \tag{4}$$

where I_S is the reverse saturation current of the diode, k is the Boltzmann constant and T is the temperature. It is interesting to study the current (I) flowing through the load if the load resistance (R_L) varied from zero (short circuit) to infinity (open circuit). Under short-circuit condition ($R_L = 0$), there is no voltage drop and the voltage (V) across the load and the diode is zero. The diode current (I_d) is therefore zero (see Eq. 4). The entire current I_L flows through the load. The short-circuit current, denoted as I_{SC} is equal to I_L ($I_{SC} = -I_L$ for $R_L = 0$, $V = 0$). As the resistance becomes finite, there is a voltage drop across the resistor. This voltage (V) increases as the resistance increases. There is then a current (I_d) through the diode (see Eq. 4). The current through the load can be written as give in Eq. 5.

$$I = I_S\left(e^{qV/kT} - 1\right) - I_L \tag{5}$$

Under open-circuit condition ($R_L = \infty$), there is no current across the load and the voltage developed only causes the current across the diode. This voltage is known as open-circuit voltage (V_{OC}) and can be determined from Eq. 5 by substituting $I = 0$ and $V = V_{OC}$. This expression is given in Eq. (6).

$$V_{OC} = (kT/q)\ln[(I_L/I_S - 1)] \tag{6}$$

This can be represented graphically as shown in Fig. 12. The current through the load (I) is a sum total of I_d and $-I_L$. The diode current is given by Eq. 4 can be drawn as per the voltage (V) across the load (and diode) and shown as I_d in Fig. 12. The photocurrent (I_L) is constant as shown. The current through the load ($I = I_d - I_L$) can be then drawn as shown in Fig. 12. The I_{SC} ($V = 0$) and V_{OC} ($I = 0$) is also shown in Fig. 12. It may be noted that the I–V characteristics appear at the fourth quadrant in which power ($P = V \times I$) is negative. This indicates the energy extracted from the device.

This I–V characteristic is an important representation of the solar cell. It is inconvenient to work always with a fourth quadrant characteristic. Therefore, for simplicity, the equivalent I–V characteristic drawn in first quadrant is used as shown in Fig. 13. Corresponding power versus voltage (P–V) characteristic is also shown. Maximum power (P_m) appears at a particular V_m known as maximum power point (MPP). The corresponding I_m is known as maximum current as shown in Fig. 13. The ideal power is the area of the rectangle defined by $V_{OC} \times I_{SC}$. However, the maximum power which can be extracted from a solar cell is the area of the rectangle defined by $V_m \times I_m$. It is to be noted that for extracting maximum power (P_m), the

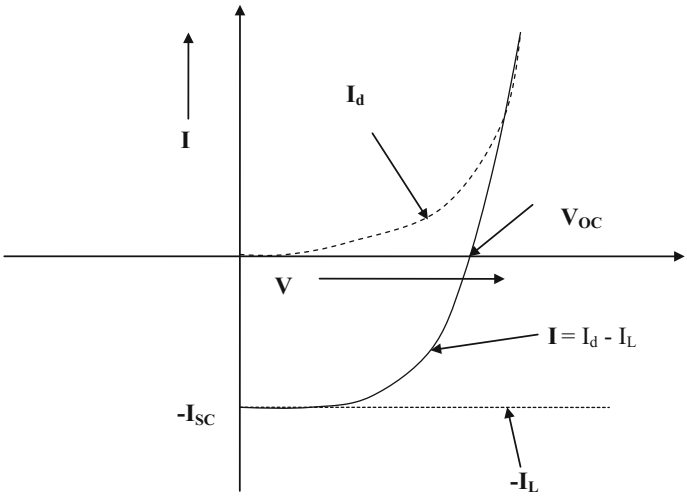


Fig. 12 I–V characteristics of a solar cell. I_d is the current through the diode, I_L is the photo-generated current, and I is the current through the load

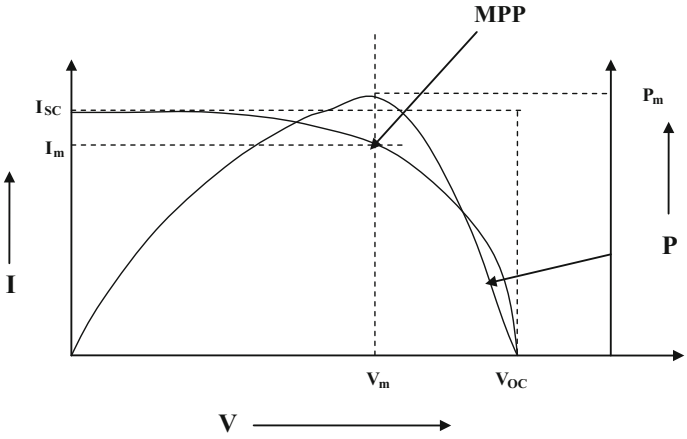


Fig. 13 Equivalent I–V drawn in first quadrant. P–V characteristic is also shown. Power is maximum at V_m (maximum voltage) and I_m (maximum current). The corresponding point is known as MPP (maximum power point)

solar cell has to be operated at MPP. The ratio between actual power and ideal power is an important parameter defined by fill factor (FF) as given in Eq. (7).

$$\mathrm{FF} = (V_m \times I_m)/(V_{OC} \times I_{SC}) \tag{7}$$

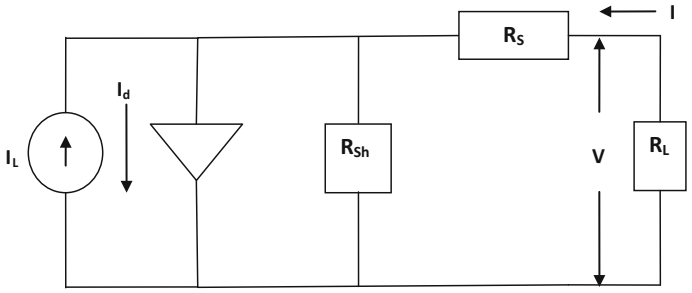


Fig. 14 Equivalent circuit of a practical solar cell with series (R_S) and shunt (R_{Sh}) resistance

The three important factors, V_{OC}, I_{SC}, and FF, together decide the power output and efficiency of a solar cell.

The equivalent circuit shown in Fig. 11 is assumed to be not affected by the internal as well as the external resistance. This is an ideal situation and not true for a practical device. There are series resistances (R_S) associated with the neutral (beyond depletion region) portion of the device material and also the external connection to be made to form the circuit. The diode has assumed to be an ideal device with infinite resistance. However, these have large but finite resistance. This resistance actually comes in parallel with the diode and the load. Therefore, this is known as shunt resistance (R_{Sh}). The equivalent circuit incorporating these resistances is shown in Fig. 14.

The current equation gets modified as given in Eq. 8.

$$I = I_S\left(e^{q(V-IRs)/kT} - 1\right) - I_L + (V + IR_S)/R_{Sh} \tag{8}$$

The I–V characteristics also get accordingly adjusted. The slopes at V_{OC} and I_{SC} move inwards reducing the fill factor. Details are not shown.

5 Solar Photovoltaic Technology

The common types of solar PV devices are shown in Fig. 15. Most of the terrestrial installations uses either c-Si or low-efficiency thin film technology such as a-Si, CIGS and CdTe. c-Si is most widely used PV technology capturing market share of about 90%. Multi-crystalline silicon (c-Si: multi) technology with efficiency range of 16–19% is more common. Higher efficiency in the range of 17–20% is achieved for monocrystalline silicon (c-Si: mono) technology. This is used mostly where there is a space constraint or space is available at premium. Both mono and multi c-Si are bulk technology which requires a silicon substrate of thickness of about 200 μm.

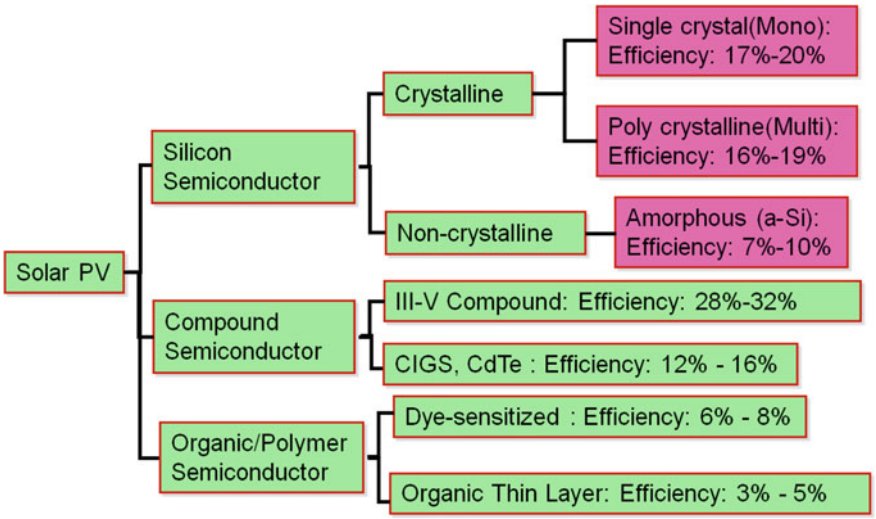


Fig. 15 Type of solar PV devices. The efficiency mentioned are stabilized efficiency and on large substrate

Thin film a-Si SPV devices are made by depositing thin layers of required materials on a glass substrate. The use of costly silicon substrate is therefore eliminated resulting in lower cost. However, the efficiency is lower (7–10%).

Other thin film technologies use materials such as CIGS and CdTe. Efficiency level of 14–16 and 12–14% are achieved for CIGS and CdTe technologies, respectively. Amongst the thin film technologies, CdTe is most commonly used and have a market share of about 10%. a-Si, which was introduced during the period when the cost of polysilicon was very high. c-Si substrates are made using polysilicon. As the prices of polysilicon came down subsequently, the a-Si technology lost its competitive advantage. CIGS technology is comparatively new amongst the thin film technologies and some recent installations are coming up. A hybrid technology, known as Heterojunction with Intrinsic Thin Layer (HIT), using combination of c-Si and a-Si thin film has been developed giving higher efficiency ($\sim$22%) [21].

Use of high-efficiency (28–32%) III–V thin film technology is not preferred in conventional terrestrial applications, except concentrated photovoltaic (CPV) systems [17, 22]. High-efficiency III–V SPV devices are used for space applications. Previously c-Si technology was used for space applications. This has now been completely replaced by the III–V technology.

Organic and polymer-based semiconductor materials are under current research. The concept has been proven and prototypes are made. Prominent amongst them are dye-sensitized solar cell (DSSC), organic thin layer solar cell [23, 24] and Perovskite solar cell [16, 25]. Solar cell technologies based on quantum mechanics [26] and nanotechnology [27] are under fundamental research.

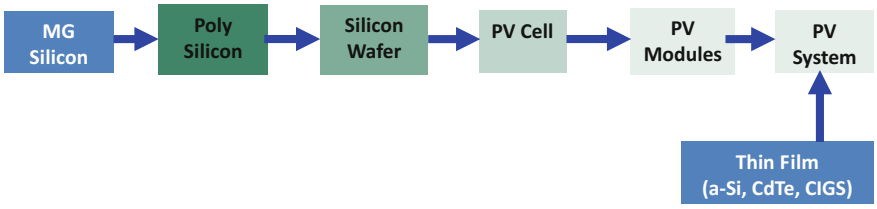


Fig. 16 Solar PV value chain

The complete solar PV value chain is shown in Fig. 16. The crystalline silicon-based solar cell has a long value chain. Each block of the value chain is a business model by itself. This starts by extracting metallurgical grade (MG) silicon from SiO_2 abundantly available in sand, quartz, etc. The MG-grade silicon is not so pure, and crystallinity level is low. This is further purified as polycrystalline silicon in the form of "chunks". The next process is crystal growth in which more pure polycrystalline, known as multi c-Si or mono-crystalline, known as mono c-Si, ingots are formed. Parallelepiped-shaped ingots are formed for multi c-Si using a die casting method. Mono c-Si in the form of cylindrical ingots is made using a more sophisticated technology such as Bridgman and Czochralsky. The respective doping (n or p-type) is done during the crystal growth process. Thin slices, of the order of 200 μm, are cut out using advanced sawing techniques. These are known as wafers. These mono or multi c-Si wafers are then used to fabricate the solar cells. The solar PV modules are then made by electrically connecting several cells in series. SPV systems are configured by connecting modules in series and parallel combinations as required.

c-Si is categorized as first-generation technology. III–V high-efficiency cells, which is primarily used for space applications and also in concentrated photovoltaic (CPV), is also in first-generation technology category. In this, the cells are made by high-quality single-crystal thin films typically using a germanium substrate. These cells are then configured directly assembled as a system as per requirement. The intermediate requirement of module manufacturing is generally skipped.

Thin film a-Si, CdTe and CIGS cells are made directly on a large substrate such a glass coated with transparent conductive oxide (TCO) such as indium tin oxide (ITO). These fall under second-generation technology. The value chain is much simpler, as shown in Fig. 16, as the cells in the size of module are directly made and several of them can be used to configure SPV system.

The third-generation technologies are dye-sensitized (DS) solar cells, organic solar cells, etc. These are yet to be matured and presently not used in commercial applications.

c-Si solar photovoltaics is the most proven and reliable technology at present. As mentioned before, the solar cells are made first, and several of them are connected together to make the modules. The cross-sectional diagram of a basic c-Si solar cell

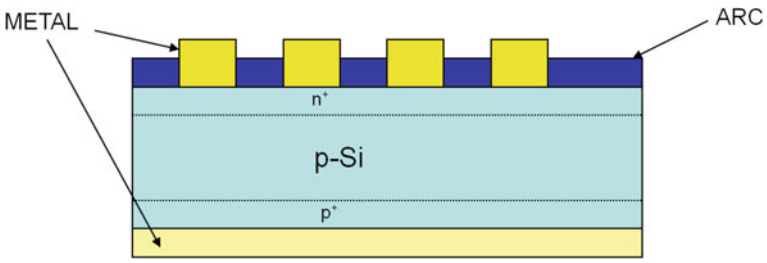


Fig. 17 Cross section of a basic solar cell

structure is shown in Fig. 17. The baseline c-Si cell manufacturing process flow is shown in Fig. 18. The c-Si solar cell is essentially a single p–n junction diode made on a single-crystal substrate. Present technology uses a 156 mm × 156 mm p-type (boron doped) silicon wafer as a substrate.

5.1 c-Si Solar Photovoltaic Technology

5.1.1 c-Si Solar Cell

Saw damage removal and texturization [28, 29] are the first step of the c-Si manufacturing process. During slicing of the ingot to take out wafers, there are damages on the surface which are to be repaired. A layer of about 10 μm is removed from the front surface where the p–n junction is formed. This is done by etching using a wet solution comprising of HF. The texturization step also uses wet solution, and this is done along with saw damage removal. Anisotropic etching in which the lateral etch rate is more than the vertical etch rate is employed to get pyramid-like structures on the surface as shown in Fig. 19. The light capture increases due to multiple reflections. Untextured and polished silicon surface have very high level of reflection. It can touch 40% which is essentially lost as it is not absorbed in the silicon bulk. Texturized surface reduces this reflection loss to as low as 4–5%. Further reduction of reflection loss is achieved through anti-reflection coating (ARC) [30, 31], which has been discussed later.

The texturization is straightforward and simpler in case of mono-crystalline silicon. Alkaline solutions such as NaOH and KOH with lower etch rate are used to form textured surface. The shape and height of the pyramids get decided by the horizontal and vertical etch rates decided by the concentration of etching solution. This gets complicated for multi-crystalline silicon as the etch rate of crystalline portion is different than that of grain boundaries. Slower etching using alkaline solutions result in irregular-shaped pyramids. Acidic solutions such as HNO_3 and HF with higher etch rates are used to circumvent this problem. However, the texturization of c-Si multi is not as good as c-Si mono. A common process for c-Si

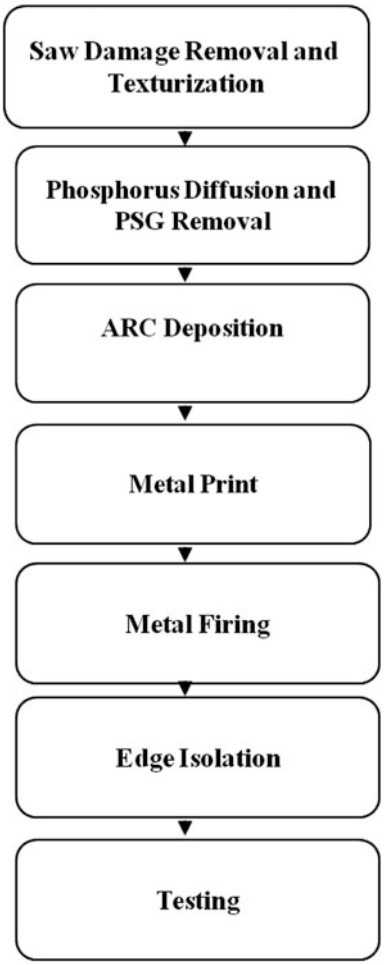


Fig. 18 Process flow of baseline c-Si cell manufacturing

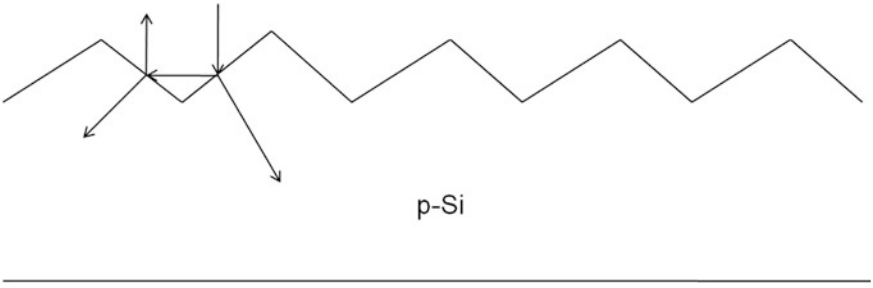


Fig. 19 Enhanced light capture due to texturized surface

mono and c-Si multi using a mixture of alkaline and acidic solution having an intermediate etch rate have been tried by researchers with limited success.

The p–n junction diode is formed by doping the top portion of the p-type substrate with phosphorus which is a n-type dopant in silicon (Fig. 17). Primarily, two processes are prevalent in solar PV industry. Dominant one uses furnace diffusion using $POCl_3$ as phosphorus-containing gas. This technique is in fact adopted from VLSI industry. $POCl_3$ along with an inert carrier gas is allowed to flow through the surface of the p-type silicon which is kept at high temperature (≈800 °C) in a furnace. The reactant gas, $POCl_3$, gets decomposed to P, O_2 and Cl_2. Phosphorus then diffuses to the silicon causing n-type doping. Alternative process, which was also been used in earlier VLSI fabrication known as pre-deposition, uses O_2 along with $POCl_3$. An intermediate compound P_2O_5 is then formed at somewhat lower temperature. This when subjected to a high temperature (800–850 °C) reacts with Si and liberates phosphorus, which acts as a n-type dopant in silicon. A complex compound ($Si_xP_yO_z$), known as phospho silicate glass (PSG), is also formed. Direct decomposition of $POCl_3$ at high temperature, skipping the intermediate pre-deposition step, is more common in solar PV industry.

An entirely different process, although less common, using spray techniques is also used for solar cell manufacturing. In this, H_3PO_4 is sprayed on the silicon substrate kept at about 200 °C. This gets decomposed in P_2O_5 and H_2O. The P_2O_5-deposited substrate is then heated at high temperature (800–850 °C) to achieve phosphorus doping similar to the alternative $POCl_3$ process. This also results forming a PSG layer on top of the substrate after completion of doping process. The PSG layer is then removed by etching using HF and H_2O_2.

As discussed earlier the reflection loss is reduced by texturization. Further, reduction of reflection loss is achieved through deposition of anti-reflection coating (ARC). Overall reflection loss of only 1–2% can be achieved with the help of ARC together with texturization. A thin film (600–800 A) of silicon nitride (Si_3N_4), deposited by plasma-enhanced chemical vapour deposition (PECVD) technique, is generally used for ARC. The refractive index (n) of Si_3N_4 ($n \approx 2$) is in between air ($n = 1$) and Si ($n \approx 4.0$). As the thickness of ARC layer falls under thin film region, interference effect decided the overall reflection loss. The refractive index along with the thickness of this thin film layer determines the interference pattern, i.e. constructive or destructive, for a particular wavelength. Destructive interference for the wavelength range of interest can be achieved by choosing appropriate thickness of Si_3N_4. The refractive index of the silicon nitride layer can also be varied by changing the stoichiometry of the film (Si_xN_y) by making either silicon reach ($n > 2$) or nitrogen reach ($n < 2$). The silicon nitride deposition is done by using SiH_4 and NH_4. The composition of these gases can be altered to get varying x and y. SiH_4 rich gas composition gives higher refractive index and vice versa. Composite ARC layers with Si_3N_4 and SiO_2 ($n = 1.4$) for better control of interference effect have also been tried.

The metal connections from the front (n) and the back (p) are required for electrical connection to the p–n diode. The front connection is not straightforward mainly due to two reasons. First, metal used for the connection typically aluminium

(Al) is opaque to the light. No light can reach silicon in case the entire front surface is covered with metal. Second problem is due to the ARC layer, which is essentially an insulator. Special process is required so that the deposited metal on the front makes electrical contact with underlying silicon. Back side metal connection has no such problems. The front side metallization is done using a paste consisting mainly of silver (Ag) along with lead and an organic binder. The composition of this metal paste is a technology by itself and is closely guarded secret kept by the suppliers.

The front metallization is done by applying the paste through a mask, typically having mesh openings, defining the fingers and the bus bars (see Fig. 20a). This is known as printing and somewhat similar to what is used in printed circuit board (PCB) process. Two-stage printing process is used to define the front and back side metals including the back bus bars. There are no fingers type patterns on the back side (see Fig. 20b). The printing process is followed by a high-temperature firing. During this step, the Pb present in metal paste dissolves the ARC layer so that Ag can make contact to underlying silicon. Front and back side of a solar cell is shown in Fig. 20. Segmented three bus bar cells are shown. Cells with four bus bars are also in use.

The final process before testing is edge isolation. During doping to make n–p junction, the phosphorus also gets doped on the sides of the cells. This can result in short between front and back side rending the n–p junction useless. A portion of the silicon is removed at the edges of the front side. The depth of etching is more than the junction depth of n^+. This removal can be done either by LASER or by chemical etching, which is more popular for current technology.

The manufactured cells are then tested in a cell tester, which record the I–V and P–V characteristics and extracts electrical parameters such as V_{OC}, I_{SC}, V_m, I_m, fill factor and power. These cells are then segregated in BINs usually in terms of power. Dedicated test set up, known as sun simulator, is used for solar cell and module testing. Some stipulated standards have to be followed, such as tester accuracy, calibration procedure for the testing.

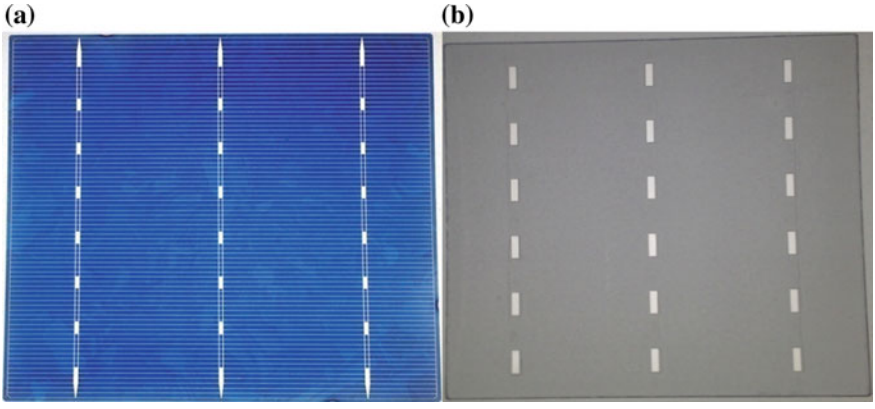


Fig. 20 **a** Front side and **b** back side of a solar cell

5.1.2 c-Si Solar Module

Several of c-Si solar cells are electrically connected, usually in series, to make a c-Si solar module. Modules with 60 cells or 70 cells connected in series are more popular. Modules with lower or higher than 60/70 cells are also available. V_{OC} of c-Si solar cell is about 0.6 V. I_{SC} depends on the efficiency of the cells and can be of the order of 9 A. As the cells are connected in series to make modules, V_{OC} of about 36 V and I_{SC} of about 9 A are achieved for a 60 cells module. Some smaller systems such as solar lantern, street light require higher voltage but less current. In such cases, "cut cells", i.e. individual cells are cut into several pieces and they are then connected in series. For example, if one c-Si cell is cut into four pieces, each piece has V_{OC} = 0.6 V and I_{SC} = 2.25 A. If these four pieces are now connected in series, V_{OC} = 2.4 V and I_{SC} = 2.25 A is achieved instead of V_{OC} = 0.6 V and I_{SC} = 9 A for one uncut cell.

Apart from the electrical connection, further processing is required to protect the c-Si cells from the external harsh environment during the operation of the modules in the field. This is achieved by lamination. The lay-up of the different layers before lamination is shown in Fig. 21. The cells are sandwiched between a front glass and a back sheet. Polymer layers made of Ethyl Vinyl Acetate (EVA) are inserted between cell string array and front glass and also between cell string array and back sheet. The cell receives the irradiance through transparent front glass as the front side of the cells face the glass. Apart from electrical connection and lamination additional process steps, such as fixing the junction box for external connection and the frame insertion for fixing the module to the external structure, are required. The module manufacturing process flow is shown in Fig. 22. An overview of various process steps are discussed below.

The electrical connection of the cells is done through an automatic process known as tabbing and stringing (T&S). Typically, a certain number of cells, e.g. 10 for 60 cells module and 12 for 72 cells module, are connected in series to make the individual strings. Required number of such strings, e.g. 6 are placed in parallel and connected in series. This process is known as bussing. The lay-up as shown in

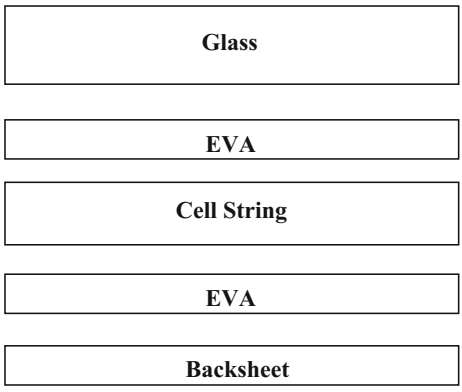


Fig. 21 Lay-up sequence of solar PV module

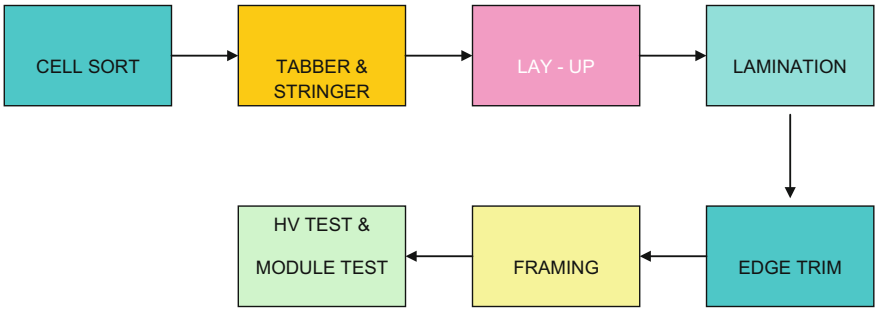


Fig. 22 Process flow of c-Si module manufacturing

Fig. 21 is then arranged. Modern manufacturing line uses automated lay-up through robotic machines. The lay-up is then laminated using an equipment called laminator. This process is in principle similar to the conventional lamination used for protecting, e.g. important documents. However, better accuracy of temperature, pressure, vacuum, etc. is needed for solar module lamination. The size of the laminator is large due to (a) large size of the module and (b) more than one module is generally laminated in one process cycle to increase the throughput. Lamination provides electrical insulation and protection of the cells from the external environment.

After lamination, the excess EVA and back sheet protruding out from sides are trimmed using a hot knife. This is known as edge trimming process. Anodized aluminium frames are then inserted from all four sides to provide strength to the module and also to make it compatible for easy installation by fixing the modules to the external frames. Double-sided tapes are inserted between the trimmed laminated module and the frame for durability. A more advanced process uses silicone glue for frame fixing. After framing, the junction box is attached to the back side of the module. The junction box connects the cell strings to external cables. It also has by-pass diodes required to optimize the power output of the module due to shading.

Finished module has to undergo detail testing for quality, safety, reliability, and performance. The quality is ensured by several quality check (QC) procedures during and after manufacturing. Reliability test is also done as per stipulated standards. One of the safety tests is the high voltage (HV) test to ensure there is no leakage between cell string and the outside conductor, such as metallic frame [32]. Electrical testing is done by measuring I–V and P–V characteristics and then extracting parameters such as P_{max}, V_{OC}, I_{SC}, V_m, I_m, fill factor. Electrical testing is carried out using dedicated tester, known as sun simulator. About 1000 W/m^2 irradiance falling perpendicular to the module kept at 25 °C is used as standard test condition (STC). The irradiance used must be equivalent to sun spectrum at AM1.5G; G denotes global. The tester must meet specific stipulated criteria such as uniformity, stability and accuracy. Calibration of the sun simulator is also important [33]. Reference modules certified by authorized agencies, such as NREL and

Fraunhofer are used for calibration. The total power obtained from a module is somewhat less than that of the sum of powers of all the cells. This is known as cell to module (CTM) conversion loss [34]. This loss must be as minimum as possible.

5.1.3 Advances in c-Si Solar PV Technology

Cell Technology

Solar PV technology has made significant advancement in last ten years. The improvement of the efficiency and reduction of cost is the hallmark of such advancement. About 10 years ago, the cost was more than $\$4/W_P$ for module. This has come down to less than $\$0.7/W_P$ due to all around advancement.

The continuous improvement of the efficiency of solar cell is one of the prime reasons for rapid progress of the solar PV. It is particularly challenging as the enhancement of the efficiency has to be done keeping the cost in mind. A brief overview of the technology advancement has been discussed next without going into much detail. The improvements of efficiency of the solar cell are achieved by (a) ensuring more light reaching silicon by reducing shading (b) increasing the probability of capturing the photo-generated carriers and (c) reduction of loss of carriers due to surface and bulk defects.

The shading loss is mainly due to the front side metal fingers and bus bars. Bus bar width and numbers are optimized based on the compatibility of the T&S process and final electrical resistance arising due to external connections. Internal series and contact resistances are decided by the widths, heights and numbers of the fingers. The width to height ratio, which is known as aspect ratio, depends on the metal printing process used. It is preferable to have smaller line width with larger height so that lower electrical resistance is achieved along with lesser shading loss. However, the aspect ratio of the conventional metal printing technology is high, requiring higher aspect ratio and results in total shading loss of about 7–9% to maintain acceptable electrical resistance. Double printing (DP) technology has recently been introduced to circumvent this issue. In this, it is possible to reduce the aspect ratio, so that the shading loss is less, typically about 4–6%, without compromising on the electrical resistance. A cross-sectional view of a metal fingerprinted in a DP technology is shown in Fig. 23b. DP uses a two-steps printing and requires a special equipment having higher accuracy, particularly for alignment of the two layers. Metal fingerprinted in conventional process is also shown in Fig. 23a for comparison. There are about 60–70 fingers in total in a typical 156 mm $\times$ 156 mm solar cell.

Shading loss can be reduced by using metal wrap through (MWT) [35] and emitter wrap through (EWT) [36] technologies. In MWT, the bus bars for front contact are placed at the back side of the cells. The shading loss due to the bus bar metal is therefore eliminated. Cross-sectional diagram of MWT process is shown in Fig. 24. Grooves are made using LASER before phosphorus diffusion step. During

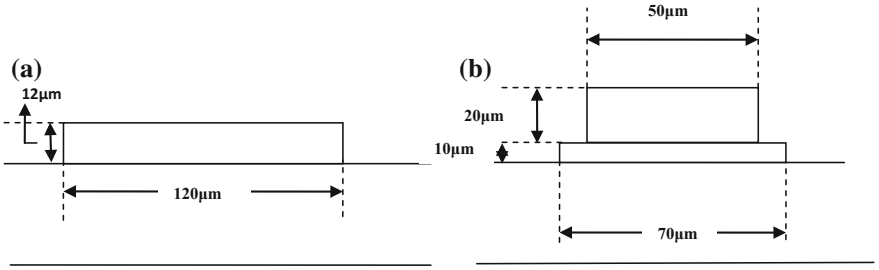


Fig. 23 **a** Conventional printing (single print) and **b** double printing technologies

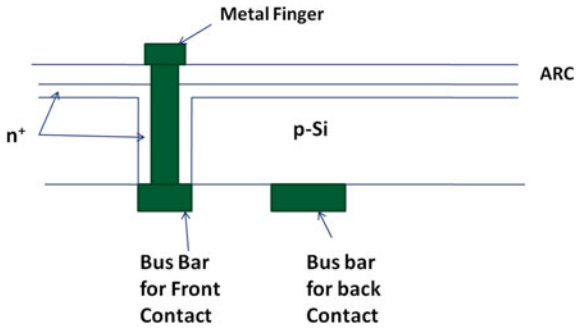


Fig. 24 Cross-sectional diagram of metal wrap through (MWT) process

the front side doping for n^+, the sides of the grooves are also doped as shown in Fig. 24. The metal fingers on the front are connected by bus bar located at the back by metal "wrap through" to the back.

In emitter wrap through (EWT) process, even the fingers are located on the back side. This eliminates the entire shading due to metal. Cross-sectional diagram of EWT process is shown in Fig. 25. Instead of metal finger, the equivalent finger connections are taken to the back side through several LASER grooves. The n^+ regions formed on the front and the sides of the grooves provide electrical connection between fingers (located at the back) and front emitter (n^+). Only one bus bar and finger have been shown in Figs. 24 and 25. There are more than one bus bar and several fingers in a solar cell. MWT and EMT processes are complex, and several details are skipped and not shown in Figs. 24 and 25. The EWT process is more complex than the MWT process.

Defect passivation [37, 38] is another area where improvements are possible. There are mainly two types of defects in crystalline materials. One is due to bulk defects such as impurities and grain boundaries. Impurities can capture active carriers resulting in reduced photocurrent. This type of defects is not very prominent for c-Si solar PV, due to high purity of substrate used to make cells. In multi-crystalline silicon, the grain boundaries are also considered as defects which can capture active carriers reducing the photocurrent. Another prominent surface defect originates due to surface state. The crystal structure is terminated at the

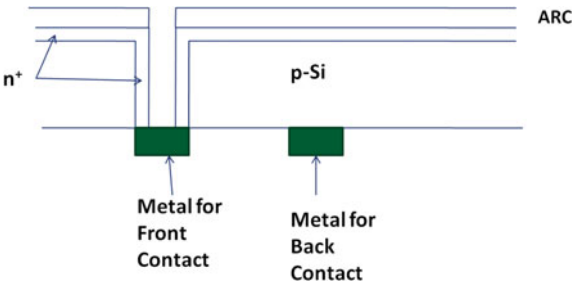


Fig. 25 Cross-sectional diagram of emitter wrap through (EWT) process

surface, and the bond structure remains incomplete for the silicon atoms located at the surface. This results in dangling bonds, which are also called surface states. These surface states can capture active carriers and reduce the photocurrent. The surface states are present both at the front and back surfaces.

The surface states can be deactivated by removing dangling bonds by providing hydrogen atoms to satisfy the incomplete silicon bonds. This technique is known as passivation and is used during several types of semiconductor device fabrication. Front surface passivation automatically happens during ARC deposition. The gasses used, SiH_4 and NH_3 for ARC deposition, contain hydrogen which can passivate incomplete silicon bonds by attaching themselves to the lattice structure. This is very effective technique and also passivates the grain boundary defects to a large extent. The same method is now being extended to back surface passivation. Additional processing steps are required to provide hydrogen to the back side for passivation. Although looks simple, it has some complications. The incorporation of hydrogen at the back silicon interferes with the p^+ doping and reduces its effectiveness. Several versions of the back surface passivation techniques have been recently developed. The simplest one is passivated emitter and rear contact (PERC) [39]. More advance techniques are passivated emitter and rear locally diffused (PERL) [40] and passivated emitter and rear totally diffused (PERT) [40]. A detail description is beyond the scope of this introductory chapter. A cross-sectional diagram of the PERT process is shown in Fig. 26. The front metal is not shown in this Figure.

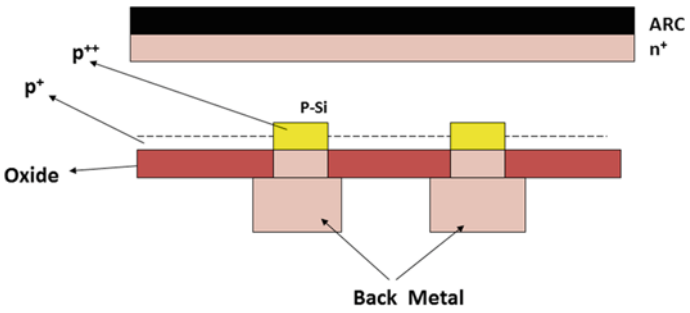


Fig. 26 Cross-sectional diagram of passivated emitter and rear totally diffused (PERT) process

Improvement of the collection efficiency of the carriers can be done by selective emitter process [41, 42]. In the conventional process (see Fig. 17), the entire surface is doped with phosphorus to form the n^+ emitter. Higher doping concentration is required to get lower resistivity and contact resistance which are prerequisite to increase the fill factor and hence the efficiency of the solar cell. However, it is known that higher doping introduces bulk defects, which act as recombination centres. The efficiency of the solar cell is thus reduced. Selective emitter introduces two separate doping regions. The portion which is connected to metal (see Fig. 27) is doped heavily to get lower electrical resistivity and contact resistance. Rest of the portion where the irradiance actually gets absorbed is doped lightly. Bulk defects arising out of doping is therefore reduced to manageable level. A cross-sectional diagram of selective emitter process is shown in Fig. 27 in which heavily doped and lightly doped regions are denoted as n^{++} and n^+, respectively.

Interdigitated back contact (IBC) [43] process has been developed to manufacture high-efficiency cells. In this, both n^+ and p^+ are formed at the back. Many closely spaced n^+ and p^+ regions are formed using lithography and ion implantation. Metal contacts are taken by opening holes, using lithography and etching, through additionally deposited oxide. The metal connections are then formed using lift-off lithography. A cross-sectional diagram of IBC process is shown in Fig. 28. The topographical pattern of IBC metal connections is shown in Fig. 29. This is a typical interdigitated pattern and hence the name IBC.

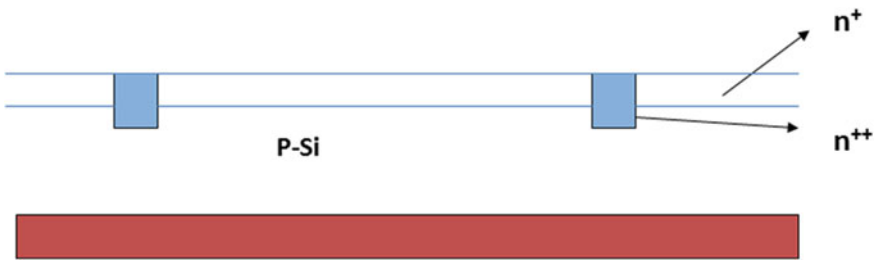


Fig. 27 Cross-sectional diagram of selective emitter process

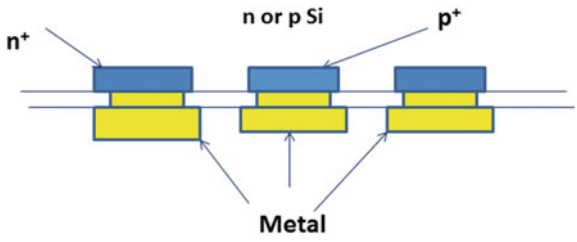


Fig. 28 Cross-sectional diagram of interdigitated back contact (IBC) process

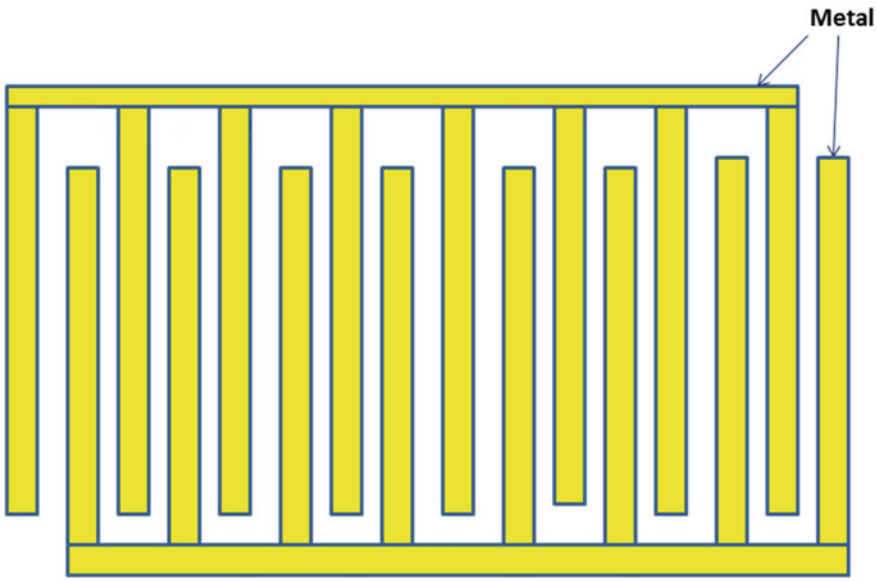


Fig. 29 Topological diagram of interdigitated back contact (IBC). Two separate comb-shaped metals connecting n^+ and p^+

There are some other advanced processes such as buried contact, light-induced electroplating that have also been developed with varying degree of success. Details are not discussed in this chapter.

Module Technology

Advances in module technology are mainly concentrated on developing new materials for cost reduction. Continuous improvement of equipment capabilities in terms of accuracy, stress reduction, and automation are also being done. Lower stress and higher automation resulted in reduction of cell thickness with very small rejection rate. Higher accuracy allows to place the cells more closer during lay-up resulting in reduction of module size giving higher effective efficiency of the module. Textured and anti-reflective-coated (ARC) glass [44, 45] have been introduced in SPV module manufacturing for improvement of the efficiency. There are some attempts for innovative process improvement [46–48] but these are limited and not very successful. Conductive adhesive instead of copper ribbon have been tried so that T&S process is replaced by a more stress-free process. There are attempt to replace the front glass by fibre-reinforced plastic (FRP) to have light-weight module. c-Si Concentrated PV (CPV) module with low level of concentration ($C < 2$) has been developed by modifying the cover glass. Instead of flat

surface, the cover glass has curved surface for concentration. Less silicon is required for producing the same power as compared to conventional module. However, these modules can only be used along with single-axis tracking system.

5.2 *Thin Film Technology*

5.2.1 a-Si, CdTe and CIGS Thin Film Technologies

Unlike c-Si; a-Si, CdTe and CIGS (Copper Indium Gallium Sulphide), thin film modules are manufactured directly by deposition techniques using transparent conductive oxide (TCO)-coated glass substrate. The process flow of a a-Si manufacturing process is shown in Fig. 30. The cross-sectional diagram of a single-junction a-Si cell is shown in Fig. 31. Plasma-enhanced chemical vapour deposition (PECVD) technique is use to deposit n–i–p layers to form the solar cell. Here, i indicate intrinsic layer. Several LASER scribing steps are used to configure these cells and also to connect, generally in parallel. Lamination step, similar to what is used for c-Si module manufacturing process, is used. However, it is common to use another glass, instead of back sheet, for lay-up and lamination. These types of modules are called glass on glass modules.

a-Si material has large number of dangling bonds. These are passivated using hydrogen, which is present in the gas (SiH_4) used for PECVD deposition of a-Si. Therefore, this material is denoted as c-Si:H. The band gap of a-Si:H is about 1.7 eV. This can be tailored by introducing C (a-Si:C) or Ge (a-Si:Ge) which have higher and lower band gap, respectively, than a-Si. It is understood that H is also present in a-Si:C and a-Si:Ge. Additional gas containing C or Ge is introduced along with main gas such as SiH_4 for formation of a-Si:C or a-Si:Ge. Multiple junction, which is also called tandem junction cells can be made by depositing

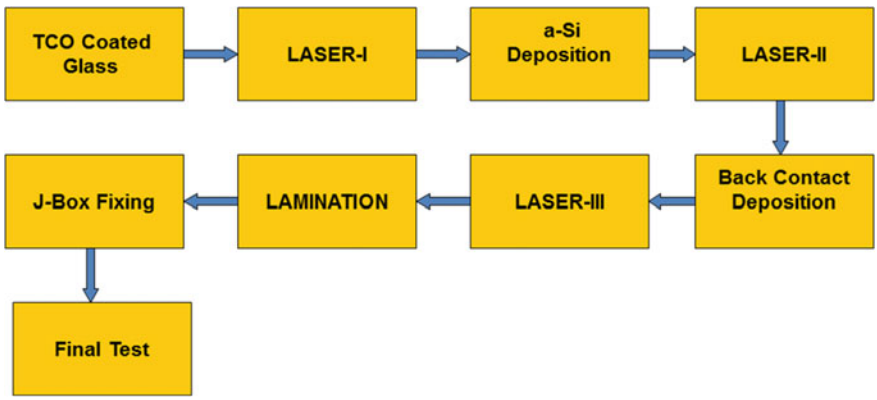


Fig. 30 a-Si thin film process flow

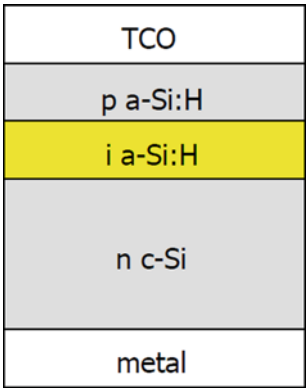


Fig. 31 Cross-sectional diagram of a single-junction a-Si thin-film solar cell

multiple layers as shown in Fig. 9. Layer 3, layer 2 and layer 1 can be made of a-Si:C, a-Si and a-Si:Ge, respectively. Band gaps of a-Si:C and a-Si:Ge can be adjusted by adjusting the amount of C and Ge present in the structure. The a-Si:Ge layer of the tandem cell can be replaced with microcrystalline silicon having band gap of about 1.1 eV. This is known as micromorph a-Si tandem solar cell. Microcrystalline layer can be formed by adjusting the deposition parameter during PECVD.

CdTe is another important thin film technology. Cross-sectional diagram is shown in Fig. 32. The process flow is somewhat similar to the a-Si solar cell. n-CdS, and p-CdTe are used for this solar cell. CdS has large band gap (≈2.42 eV) and therefore acts as a window for incoming light. Most of the light spectrum is absorbed in p-CdTe having a band gap of about 1.45 eV which is very close to the ideal band gap (see Fig. 8).

CIGS solar cell is relatively new technology which also uses the similar process as a-Si and CdTe. The cross-sectional diagram is shown in Fig. 33. In this also CdS is used as window layer.

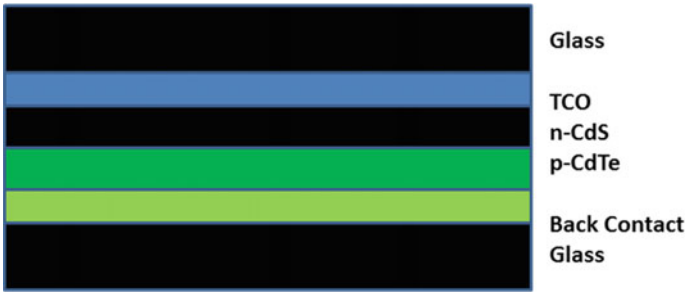


Fig. 32 Cross-sectional diagram of a CdTe thin-film solar cell

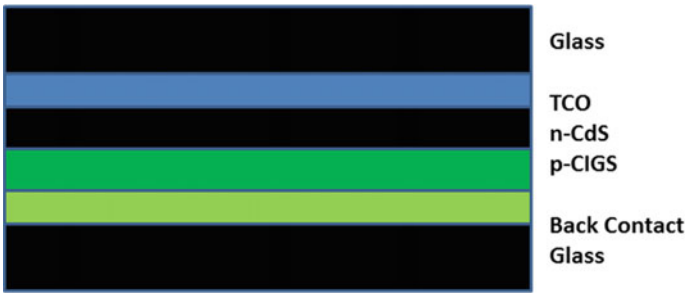


Fig. 33 Cross-sectional diagram of a CIGS thin-film solar cell

5.3 High-Efficiency III–V Solar Cell Technology

High-efficiency III–V cells [49] are used in space and terrestrial CPV applications. It is not preferred in conventional terrestrial application due to higher cost. It is possible to tailor the band gap by using ternary or quaternary compounds as discussed in Sect. 3. A cross-sectional diagram of a triple-junction high-efficiency solar cell is shown in Fig. 34. Germanium, which has close lattice matching with III–V compounds, is used as a substrate. Any III–V compound such as GaAs is a better option, but to reduce the cost Ge is used. High-quality single-crystal thin film

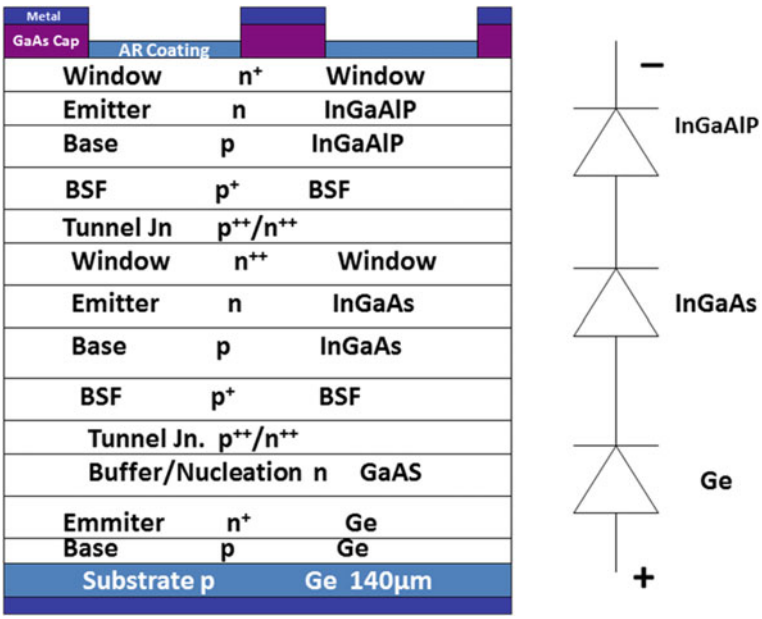


Fig. 34 Cross-sectional diagram of a III–V high-efficiency triple-junction solar cell. The diode representation of this triple-junction cell is also shown on the right

layers are deposited on the substrate usually using metal-organic vapour phase epitaxy (MOVPE) [50]. Figure 34 shows the layer sequence and composition. Other combinations are also possible. Lithography and etching steps are used to define the structure. The gasses and the processes employed are expensive resulting in higher cost of III–V high-efficiency cells. The MOVPE equipment is also very expensive and has lower throughput, adding to the overall cost. The laboratory scale efficiency achieved for triple-junction III–V cell is more than 40%. Commercial cells have achieved maximum efficiency of about 32% at present.

Similar to c-Si technology, III–V cells having diameter of about 100 mm are made first. These cells are then connected together to get a bigger system such as module. In this case, however, there is no standard module size. The cells are assembled directly on the final system such as solar panel for the spacecraft. In terrestrial applications, the cells are cut into small pieces and then assembled along with the concentrator, usually made of large lenses, to configure a CPV system.

5.4 Dye-Sensitized Solar Cell (DSSC)

Details of third-generation cell technologies are not taken up as the focus of this chapter is more on the commercial technologies. A brief description of DSSC is given in this section to bring out some basic understanding of such technologies.

Photosensitive dye such as ruthenium polypyridine dissolved in a suitable solvent is used in DSSC. The dye is coated with TiO_2 nano-particles of about 2 nm in size (diameter). These are immersed in an electrolyte, typically made of compounds of iodine dissolved in solvent such as acetonitrile (Fig. 35). Fluorine-doped Tin Oxide (FTO), which has a high conductivity, is used as one of the electrodes. FTO is transparent and allows the light to enter the cell. The other electrode uses a coating of platinum or carbon which also acts as a catalyst. During exposure with light, photons are absorbed by the dye and electrons and holes are produced as shown in Fig. 36. The electrons are moved to the TiO_2 conduction band (Fig. 36) and travel to the other side of the electrolyte through FTO, load and opposite electrode (Fig. 35). The holes get neutralized by the negative ions in the electrolyte. The negative ions are typically negatively charged iodide (I^-) or tri-iodide (I_3^-). The loss of negative charges in iodide gets compensated by the electrons entering the electrolyte from the opposite side of the transparent electrode. The coating of platinum or carbon acts as a catalyst to help the conversion of iodide or tri-iodide to negative ions. The electron flowing through the load produces current which is similar to short-circuit current (I_{SC}) if $R_L = 0$. The open-circuit voltage (V_{OC}) gets decided by the potential difference between the conduction band of TiO_2 and the negative ion. The negative ion potential is also known as redox potential.

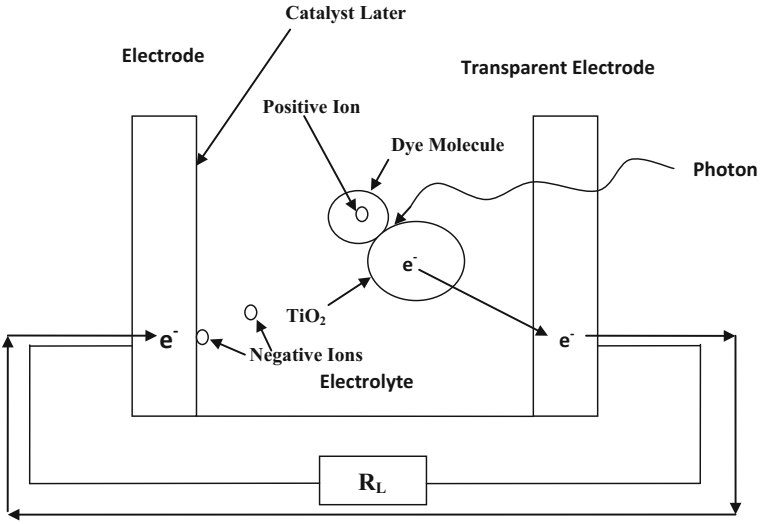


Fig. 35 Representative structure of dye-sensitized solar cell (DSSC)

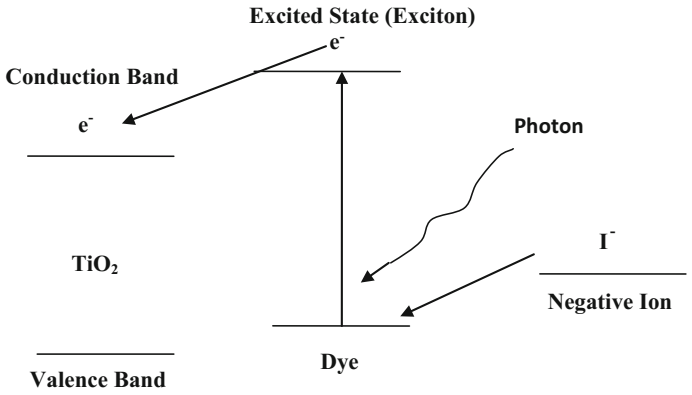


Fig. 36 Energy levels applicable to dye-sensitized solar cell (DSSC)

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